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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/875,197 | 06/07/2001 | Joon-Young Yang | 8733.132.20 | 8761 |

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| EXAMINER | |
|---|---|
| RAO, SHRINIVAS H | |
| ART UNIT | PAPER NUMBER |
| 2814 | |

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/875,197 | YANG, JOON-YOUNG | |
| | Examiner | Art Unit | |
| | Steven H. Rao | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on 23 October 2003.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 41-56 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 41-56 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 15.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

***Response to Amendment***

Applicants' amendment filed on October 01, 2003 has been forwarded on October 23, 2003.

Therefore claims 41 and 55 as amended by the amendment and claims 42-54 and 56 as previously recited are currently pending in the Application.

Claims 1 to 40 were previously cancelled.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 41-54 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicants' have amended claims 41 to include, " whereby a post heat treatment for activation of the impurity ions is eliminated from the method of fabricating thin film transistor" . the specification as originally filed does not describe / support disclosure of the process wherein a post heat treatment for activation of the impurity ions is eliminated from the method of fabricating thin film transistor, for example see specification pages 3 lines 14-15, page 6 lines 8-10 and page 6 lines 20-26.

Applicants' specification page 6 lines 20-24 describing figure 2 B states: " Subsequently, the exposed surface of the active layer 35 collided with the implanted hydrogen ions is heated to the optimal temperature range falling between 200 –300 degrees Celsius, thereby forming an excited region 41, as illustrated in Fig. 2B. ( emphasis supplied).

Claims 42-54 are rejected at least for depending upon rejected claim 41.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 41-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi ( U.S. Patent No. 5,897,346, herein after Yamamguchi).

With respect to claim 41 Yamaguchi describes a method of fabricating a thin film transistor, comprising: forming a gate insulating layer on an active layer (Yamaguchi fig. 1B # 13, col. 8 line2 and fig. 1C # 14); forming a gate on the gate insulating layer; forming an excited region in an exposed portion of the active layer by implanting hydrogen ions to the active layer by using the gate as a mask (figs. 1 C and A); and forming an impurity region by heavily implanting impurity ions to said excited region while the excited region remains in an excited state, ( Fig. 1 C implanting P+ ions ).

It is noted that Yamaguchi discloses the use of active layer as a mask and implanting prior to the formation of the gate. However it would be an obvious altering of

the sequence of steps to implant the H after gate formation. Further as Applicants' claims use the terminology " comprising" the claim includes steps in any sequence .

"Whereby a post heat treatment for activation of the impurity ions is eliminated from the method of fabricating the thin film transistor ".

Assuming arguendo that Applicants' some how over come the 122 new matter rejection. ( Yamaguchi col. 8 lines 25 , heating at about 300 degrees similar/identical to Applicants' disclosure of heating between 200—300 degrees, see above).

With respect to claim 42 Yamaguchi describes the method of claim 41, wherein the gate insulating layer is formed by depositing silicon dioxide or silicon nitride on a glass substrate. ( Yamaguchi col. 8 line 2).

With respect to claim 43 Yamaguchi describes t he method of claim 41, wherein the active layer is formed by depositing undoped polycrystalline silicon. ( Yamaguchi col. 7 line 50).

With respect to claim 44 , Yamaguchi describes the method of claim 43, wherein the undoped polycrystalline silicon has a thickness of between about 400 and 800 A. ( Yamaguchi col. 7 line 47).

With respect to claim 45 Yamaguchi describes the method of claim 43, wherein the active layer is formed using chemical vapor deposition process. ( Yamaguchi col. 7 line 48)

With respect to claim 46 Yamaguchi describes the method of claim 41, wherein the active layer is formed by depositing amorphous silicon and crystallizing the amorphous silicon by laser annealing. ( Yamaguchi col. 7 lines 46-51).

With respect to claim 47, Yamaguchi describes the method of claim 41, wherein the exposed portion of the active layer is formed by the steps of depositing an another layer of silicon dioxide on the gate insulating layer to cover the active layer; depositing a conductive material on the another layer of silicon dioxide; and patterning the conductive material and the another layer of silicon dioxide to form an insulating layer and to form the gate over a selected portion of the active layer. ( Yamaguchi Fig. 3 E).

With respect to claim 48 Yamaguchi describes the method of claim 47, wherein the gate insulating layer and the gate comprise a thickness of about 500-1500 A and, about 1500-:2500 A, respectively. ( Yamaguchi col. 8 lines 2 and 5).

With respect to claim 49 Yamaguchi describes the method of claim 41, wherein said hydrogen ions are implanted with implantation energy between about 50 and 150 KeV. ( Yamaguchi col. 9 line 15).

With respect to claim 50 Yamaguchi describes the method of claim 41, wherein said hydrogen ions are implanted with a dose of between about $5 \times 10^{14}$ - $5 \times 10^{16}$ ions/$cm^2$ ( Yamaguchi col. 9 line 14).

With respect to claim 51 Yamaguchi describes the method of claim 49, wherein said hydrogen ions are implanted to heat up the excited region to a temperature between about 200-300 degrees Celsius. ( Yamaguchi col.9 line 15 and 54).

With respect to claim 52 Yamaguchi describes the method of claim 50, wherein said hydrogen ions are implanted to heat up the excited region to a temperature between about 200-300 degrees Celsius. ( Yamaguchi col.9 line 15 and 54).

With respect to claim 53, Yamaguchi describes the method of claim 41, wherein said hydrogen ions are implanted in the active layer and simultaneously form the impurity region. ( It is inherent when a dopant is implanted an impurity region is formed).

With respect to claim 54, Yamaguchi describes the method of claim 41, wherein the hydrogen ion implantation time is proportionately related to the size of the active layer. ( Inherent because bigger the area the longer it will take).

With respect to claim 55, Yamaguchi describes a thin film transistor prepared by a process comprising: forming a gate insulating layer on an active layer; forming a gate on the gate insulating layer; forming an excited region in an exposed portion of the active layer by implanting hydrogen ions to the active layer by using the gate as a mask; and forming an impurity region by implanting impurity ions to said excited region while the excited region remains in an excited state, wherein the activation of said impurity ions implanted heavily occurs as the step of said implanting impurity ions is performed. ( rejected for same reasons as claim 41 above).

By the present amendment Applicants' have deleted the word" heavily" occurring before "implanting impurity" from line 6 and 'heavily" from line 9 , as the previously referred to sections of Yamaguchi ( col. 9 lines 14 and figs. 1C, etc. describe heavily implanting ions, they also describe implanting ions).

Wit respect to claim 56 Yamaguchi describes the thin film transistor of claim 55, wherein the, gate insulating layer is formed by depositing silicon dioxide or silicon nitride

on a glass substrate, and the active layer is formed by depositing undoped polycrystalline silicon. ( rejected for same reasons as claim 42).

***Response to Arguments***

Applicant's arguments filed on 10/23/03 have been fully considered but they are not persuasive for the following reasons.

Applicants' first contention that Yamaguchi allegedly does not describe ," forming an impurity region by implanting impurity ions to said excited region while the excited region remains in excited state," is not persuasive because see Yamaguchi figs. 1C and A, fig. 1C implanting P+ ions.

The recitation< " whereby a post heat treatment for activation of the impurity ions is eliminated from the method of fabricating the thin film transistor" is new matter as said above and has not be entered and cannot be given patentable weight.

Applicants' second contention that claim 55 is allowable because Yamaguchi fails to teach teaches the recited steps, " forming an impurity region by implanting impurity ions to said excited region while the excited region remains in an excited state, wherein the activation of said impurity ions implanted occurs as the step of said implanting impurity ions is performed" is not persuasive because see Yamaguchi figs. 1C and A, fig. 1C implanting P+ ions, and col. 8 lines 24-25 describe the activation occurring while the implanting is performed.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H Rao whose telephone number is (703) 306-5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

Dec. 26, 2003.

LONG PHAM
PRIMARY EXAMINER